What is claimed is:

1. A method of fabricating an integrated circuit, the method comprising:

forming an isolation trench, having a bottom and sidewalls, in a semiconductor substrate;

partially filling the trench with a dielectric material so that the sidewalls and the bottom of the trench are coated with the dielectric material; and

implanting ions into the substrate in regions directly below the isolation trench after partially filling the trench with the dielectric material.

2. The method of claim 1 wherein implanting ions into the substrate includes bombarding the substrate with ions at an energy such that the dielectric material along the sidewalls of the trench serves as a mask that prevents ions from becoming implanted in an area of the substrate directly below the sidewalls.

3. The method of claim 1 further including filling the trench with a dielectric material after the ions are implanted in the substrate below the trenches.

4. The method of claim 1 wherein substantially all of the ions implanted below the isolation trench are displaced horizontally from sidewall edges of the trench.

5. The method of claim 1 wherein partially filling the trench includes growing an oxide material.

6. The method of claim 1 wherein partially filling the trench includes growing a layer of silicon dioxide.

7. The method of claim 1 wherein partially filling the trench includes depositing the dielectric material by chemical vapor deposition.

8. The method of claim 1 wherein partially filling the trench includes thermally growing the dielectric material.

9. The method of claim 1 wherein partially filling the trench includes:

thermally growing a dielectric material; and

depositing an dielectric material by chemical vapor deposition.

10. The method of claim 1 wherein the dielectric material has a sidewall thickness less than about forty percent the width of the trench.

11. The method of claim 1 wherein the dielectric material has a thickness of at least about one hundred angstroms.

12. The method of claim 1 wherein implanting ions includes implanting ions of a particular type of conductivity into regions of the substrate having the same type of conductivity.

13. The method of claim 1 wherein implanting ions includes performing a shallow implant to establish a field threshold voltage.

14. The method of claim 1 wherein implanting ions includes performing an implant whose depth into the

substrate is greater than the thickness of the dielectric material at the bottom of the trench.

15. The method of claim 14 wherein the implant has a depth into the substrate which is in a range of about 10 to 100 percent the depth of the trench.

16. The method of claim 14 wherein the implant has a depth into the substrate which is in a range of about 20 to 80 percent the depth of the trench.

17. The method of claim 1 wherein implanting ions includes:

performing a shallow implant to establish a field threshold voltage; and

performing an implant whose depth into the substrate in a range of about 10 to 100 percent of the trench depth.

18. A method of fabricating an integrated circuit having a plurality of active regions separated by field isolation regions, the method comprising:

etching the substrate to form trenches separating the active regions from one another;

partially filling each trench with a first dielectric material so that sidewalls of the trench are covered with the dielectric;

directing ions at an upper surface of the substrate after partially filling the trenches with the dielectric material so that ions are implanted in regions of the substrate below the partially-filled trenches; and

substantially filling unfilled portions of the trenches with a second dielectric material after the ions are implanted in the substrate below the trenches.

19. The method of claim 18 wherein partially filling each trench with a dielectric material includes forming a dielectric layer whose thickness is substantially conformal.

20. The method of claim 19 wherein forming a dielectric material includes depositing the dielectric material by chemical vapor deposition.

21. The method of claim 19 wherein forming a dielectric material includes thermally growing the dielectric material.

22. The method of claim 19 wherein forming a dielectric material includes:

thermally growing an oxide material; and

depositing an oxide material by chemical vapor deposition.

23. The method of claim 18 wherein partially filling each trench with a dielectric material includes forming a dielectric layer over substantially an entire upper surface of the substrate, wherein the dielectric layer has an average thickness in regions above the active regions that is greater than its average thickness in the trenches.

24. The method of claim 23 wherein forming a dielectric material includes depositing a dielectric material by chemical vapor deposition.

25. The method of claim 22 wherein forming a dielectric material includes:

thermally growing an oxide material; and

depositing an oxide material by chemical vapor deposition.

26. The method of claim 18 wherein partially filling each trench with a dielectric material includes providing a dielectric material along sidewalls of the trench such that a sidewall thickness of the dielectric material is less than about forty percent the width of the trench.

27. The method of claim 18 wherein partially filling each trench with a dielectric material includes providing a dielectric material having a thickness of at least about one hundred angstroms.

28. The method of claim 18 wherein directing ions at an upper surface includes implanting ions of a particular type of conductivity into regions of the substrate having the same type of conductivity.

29. The method of claim 18 wherein directing ions at an upper surface includes performing a shallow implant to establish a field threshold voltage.

30. The method of claim 18 wherein directing ions at an upper surface includes performing an implant whose depth into the substrate is greater than the thickness of the dielectric material at the bottom of the trench.

31. The method of claim 30 wherein the implant has a depth into the substrate which is in a range of about 10 to 100 percent the depth of the trench.

32. The method of claim 30 wherein the implant has a depth into the substrate which is in a range of about 20 to 80 percent the depth of the trench.

33. The method of claim 18 wherein implanting ions includes:

performing a shallow implant to establish a field threshold voltage; and

performing an implant whose depth into the substrate in a range of about 10 to 100 percent of the trench depth.

34. A method of fabricating a device having a plurality of active regions separated by field isolation regions, the method comprising:

forming impurity-doped regions in the active regions;

forming isolation trenches in the substrate to separate the active regions from one another;

partially filling each trench with a dielectric material so that at least sidewalls of the trench are coated with the dielectric;

implanting ions in regions of the substrate below the trenches after partially filling the trenches with the dielectric material; and

substantially filling unfilled portions of the trenches with a dielectric material after the ions are implanted in the substrate below the trenches.

35. The method of claim 34 wherein implanting ions includes performing a shallow implant to establish a field threshold voltage.

36. The method of claim 34 wherein implanting ions includes performing an implant whose depth into the substrate is greater than the thickness of dielectric material at the bottom of the trench.

37. The method of claim 36 wherein the implant has a depth into the substrate which is in a range of about 10 to 100 percent the depth of the trench.

38. The method of claim 36 wherein the implant has a depth into the substrate which is in a range of about 20 to 80 percent the depth of the trench.

39. The method of claim 34 wherein implanting ions includes:

performing a shallow implant to establish a field threshold voltage; and

performing a deep implant whose depth into the substrate is in the range of about 10 to 100 percent the depth of the trench.

40. The method of claim 34 wherein forming impurity-doped regions in the active regions includes forming storage nodes for a memory device.

41. The method of claim 34 wherein forming impurity-doped regions in the active regions includes forming photosensitive elements for an imaging device.

42. The method of claim 34 wherein forming impurity-doped regions in the active regions includes forming active elements for a logic device.

43. An integrated circuit comprising:

a semiconductor substrate including a plurality of active regions; and

a field isolation region separating active regions;

wherein the field isolation region includes an area filled with dielectric material, wherein ions are implanted in a region of the semiconductor substrate directly below the dielectric material and wherein substantially all the ions are displaced away from the active regions.

44. The integrated circuit of claim 43 wherein the area filled with dielectric material includes first dielectric regions forming sidewalls of the dielectric-filled area, wherein ions are implanted in a region of the semiconductor substrate directly below the dielectric-filled area and wherein substantially all the ions are displaced from the active regions by a distance approximately equal to a sidewall thickness of the first dielectric regions.

45. The integrated circuit of claim 43 wherein substantially all the ions are displaced from the active regions by at least one hundred angstroms.

46. The integrated circuit of claim 43 wherein the active regions include elements of a memory device.

47. The integrated circuit of claim 43 wherein the active regions form photosensitive pixels.

48. The integrated circuit of claim 43 wherein the active regions form logic devices.

49. The integrated circuit of claim 43 wherein the implanted ions have a conductivity type the same as the substrate.

50. The integrated circuit of claim 43 wherein the implanted ions establish a field threshold voltage.

51. The integrated circuit of claim 43 wherein the ions are implanted into the substrate below the dielectric-filled area to a depth in a range of about 10 to 100 percent the depth of the dielectric-filled area.

52. The integrated circuit of claim 43 wherein the ions are implanted into the substrate below the dielectric-filled area to a depth in a range of about 20 to 80 percent the depth of the dielectric-filled area.

53. A memory device comprising:

a semiconductor substrate including a plurality of impurity-doped regions serving as memory storage nodes;

a field isolation region separating adjacent storage nodes; and

capacitive cells provided above the field isolation region;

wherein the field isolation region includes an area filled with dielectric material including first dielectric regions forming sidewalls of the dielectric-

filled area, wherein ions are implanted in a region of the semiconductor substrate directly below the dielectric-filled area and wherein substantially all the ions are displaced from the active regions by a distance approximately equal to a sidewall thickness of the first dielectric regions.

54. The memory device of claim 53 wherein the implanted ions establish a field threshold voltage.

55. The memory device of claim 53 wherein the sidewall thickness of the first dielectric regions is less than about forty percent the width of the isolation region.

56. The memory device of claim 55 wherein the first dielectric material has a sidewall thickness of at least about one hundred angstroms.

57. The memory device of claim 53 wherein the implanted ions have a conductivity type the same as the substrate.

58. The memory device of claim 53 wherein the implanted ions establish a field threshold voltage.

59. The memory device of claim 53 wherein the ions are implanted into the substrate below the dielectric-filled area to a depth in a range of about 10 to 100 percent the depth of the dielectric-filled area.

60. The memory device of claim 53 wherein the ions are implanted into the substrate below the dielectric-filled area to a depth in a range of about 20 to 80 percent the depth of the dielectric-filled area.

61. An imaging device comprising:

a semiconductor substrate including a plurality of photosensitive pixels; and

a field isolation region separating adjacent pixels;

wherein the field isolation region includes an area filled with dielectric material including first dielectric regions forming sidewalls of the dielectric-filled area, wherein ions are implanted in a region of the semiconductor substrate directly below the dielectric-filled area and wherein substantially all the ions are displaced from the active regions by a distance approximately equal to a sidewall thickness of the first dielectric regions.

62. The imaging device of claim 61 wherein a sidewall thickness of the first dielectric regions is less than about forty percent the width of the isolation region.

63. The imaging device of claim 61 wherein the implanted ions establish a field threshold voltage.

64. The imaging device of claim 61 wherein the ions are implanted into the substrate below the dielectric-filled area to a depth in a range of about 10 to 100 percent the depth of the dielectric-filled area.

65. The imaging device of claim 61 wherein the ions are implanted into the substrate below the dielectric-filled area to a depth in a range of about 20 to 80 percent the depth of the dielectric-filled area.

66. The imaging device of claim 61 wherein the implanted ions include:

shallowly implanted ions that establish a field threshold voltage; and

ions implanted to a depth into the substrate which is in a range of about 10 to 100 percent the depth of the dielectric-filled area.

67. The imaging device of claim 61 wherein the implanted ions have a conductivity type the same as the substrate.

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